UNITED STATES PATENT AND TRADEMARK OFFICE

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10/554,398	11/15/2006	Masayoshi Son	280102US2XPCT	4616

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EXAMINER
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ART UNIT	PAPER NUMBER
2111	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>24 October 2005</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-7</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-7</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

1.   Claims 1 – 7 are pending.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3.   Claims 1 – 3,5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mowery et al (US7136950) hereinafter Mowery in view of Huang et al (US20020111771) herein after Huang in view of Petty (US6389486).

4.   As to claims 1, and 5, Mowery discloses A PC card having a connection plug connectable to an information processing apparatus, and a card connector through which an additional card can be connected, wherein multiple capabilities are added to said information processing apparatus by connecting said PC card to said information processing apparatus, said PC card comprising: a communication control unit configured to control communication between said information processing apparatus and a function control unit of said PC card, and communication between said information processing apparatus and a function control unit of raid additional card (Figure 1 illustrates a system comprising of a PCI bus that couples PC card controller , which is coupled to another controller card such as media interface card 120, COL. 2, lines 13 – 33) ; and an area builder unit configured to analyze a card information

structure of said additional card, build a global card information structure from the card

information structure of said additional card together with a card information structure of

said PC card, analyze card configuration information of said additional card, and build a

global register area from the card configuration information of said additional card

together with a card configuration information of said PC card.

However, Huang teaches an area builder unit configured to analyze a card

information structure of said additional card, build a global card information structure

from the card information structure of said additional card together with a card

information structure of said PC card, analyze card configuration information of said

additional card, and build a global register area from the card configuration information

of said additional card together with a card configuration information of said PC card as

illustrated in Figure 9. Said figure illustrates the logic and registers to manage to

plurality of interfaces it need to control, page 5, paragraph 0060.

It would have been obvious to one of ordinary skill in the art at the time of the

invention to use the control logic of Huang in the system of Mowery to manage the

plurality of expansion cards, page 1, paragraph 0002.

Mowery as modified by Huang does not explicitly disclose   recognize memory space of

said PC card and memory_ space of said additional card.

However, Petty teaches of recognize memory space of said PC card and memory_

space of said additional card as illustrated in Figure 5. Said figure illustrates a system

comprising host pc and add on card controller with the capability of writing CIS

information to SRAM dependent on ownership. It would have been obvious to one of

ordinary skill in the art at the time of the invention to use the scheme of Petty in the

system of Mowery/Huang to allow for the successful interchanging of memory cards into

data systems, COL. 1, lines 43 – 53. One of ordinary skill in the art would have been

motivated to use the scheme of Petty in the system of Mowery/Huang to allow for the

successful interchanging of memory cards into data systems, COL. 1, lines 43 – 53.

Petty teaches an area builder unit configured to analyze a card information

structure of said additional card, build a global card information structure from the card

information structure of said additional card recognize the location of an attribute area

for storing card property information and card configuration information in the memory

space of each of said PC card and said additional card, build a global card information

structure area and a global register area in the attribute area of said PC card, locate the

card information structure of said additional card in said global card information

structure area together with a card information structure of said PC card, analyze card

configuration information of said additional card, and build a global register area from

the card configuration information of said additional card and perform an address

control operation in order to locate the card configuration information of said additional

card in said global register area together with a card configuration information of said

PC card (Figure 7 illustrates the steps involved in configuring the controlling CIS

information from either the host device, or the peripheral card in steps 102 through 116,

COL. 6, line 63 – COL. 7, line 30).

Petty teaches wherein said area builder unit performs said address control operation when power is supplied to said PC card, and said communication control unit transmits an initialization completion notification signal, which notifies that said card information structure is ready for reading, when said address control operation is completed (Figure 7, step 114 with an affirmative response, Col. 7, lines 10 – 15).

5.   As to claims 2 and 6, Huang discloses the PC card further comprising an address control unit configured to switch address operations in order that a functional register group of said PC card is located in an I/O area of said PC card when said information processing apparatus outputs an I/O area control signal for accessing the function of said PC card, and that a functional register group of said additional card is located in the I/O area of said PC card when said information processing apparatus outputs an I/O area control signal for accessing the function of said additional card (Determination of which port will be enabled, page 6, paragraph 0062).

6.   As to claims 3 and 7, Huang discloses the PC card further comprising an interrupt request control unit that, when an interrupt request is received from the function control unit of said PC card or the function control unit of said additional card, sets information about said interrupt request in an interrupt cause register (Figure 10 , step 1006 enables a certain slot to be active, page 6, paragraph 0064).

7.   Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mowery

in view of Huang in further view of Petty, and in further view of Sakurai (US6832104).

8.   As to claim 4, Mowery as modified by Huang does not discloses the PC card

wherein the function control unit of said PC card is provided with a wireless LAN

communication capability, and the function control unit of said additional card is

provided with a PHS communication capability.

However, Sakurai teaches the PC card wherein the function control unit of said

PC card is provided with a wireless LAN communication capability, and the function

control unit of said additional card is provided with a PHS communication capability

information device with PHS capability taught, COL. 1, lines 13 – 26.

It would have been obvious to one of ordinary skill in the art at the time of the invention

to have the full features of Sakurai in the system of Mowery/Huang/Petty to support

wireless networks anywhere, COL. 1, lines 47 – 56. One of ordinary skill in the art

would have been motivated to embed the full features of Sakurai in the system of

Mowery/Huang/Petty to support wireless networks anywhere, COL. 1, lines 47 – 56.

Sakurai teaches said card configuration information is information required for activating

said PC card and said additional card including a drive voltage level for said wireless

LAN capability and PHS communication capability (Figure 10, steps S1001 and S1002

enable the signal to enable the requisite interface, COL. 11, lines 33 – 50).

Response to Arguments

9.   Applicant's arguments with respect to claims 1,4, and 5 have been considered

but are moot in view of the new ground(s) of rejection.

The Applicant has argued that "In response the Applicant's argument, the

Examiner points to the teaching of Petty. Petty teaches of recognize memory space of

said PC card and memory_ space of said additional card as illustrated in Figure 5. Said

figure illustrates a system comprising host pc and add on card controller with the

capability of writing CIS information to SRAM dependent on ownership. It would have

been obvious to one of ordinary skill in the art at the time of the invention to use the

scheme of Petty in the system of Mowery/Huang to allow for the successful

interchanging of memory cards into data systems, COL. 1, lines 43 – 53. One of

ordinary skill in the art would have been motivated to use the scheme of Petty in the

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Petty teaches an area builder unit configured to analyze a card information

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space of each of said PC card and said additional card, build a global card information

structure area and a global register area in the attribute area of said PC card, locate the

card information structure of said additional card in said global card information

structure area together with a card information structure of said PC card, analyze card

configuration information of said additional card, and build a global register area from

the card configuration information of said additional card and perform an address

control operation in order to locate the card configuration information of said additional

card in said global register area together with a card configuration information of said

PC card (Figure 7 illustrates the steps involved in configuring the controlling CIS

information from either the host device, or the peripheral card in steps 102 through 116,

COL. 6, line 63 – COL. 7, line 30).

Petty teaches wherein said area builder unit performs said address control

operation when power is supplied to said PC card, and said communication control unit

transmits an initialization completion notification signal, which notifies that said card

information structure is ready for reading, when said address control operation is

completed (Figure 7, step 114 with an affirmative response, Col. 7, lines 10 – 15). Thus

the prior art clearly teaches the feature claimed.

With regards to the Applicant's argument that prior art does not teach"

An advantageous feature of Applicants' initialization completion notification signal

is that a problem of the PC being unable to recognize other cards with the initial state

address structure when the power supply is initialized is solved due to the cards each

having an information processing function and being connected serially. In contrast,

describes a parallel connection which technically differentiates the need for an

initialization completion notification signal because of register controls. This parallel

connection requires an altogether different method for control logic described by Huang

during the 'power on' state 5 Therefore, Applicants respectfully submit that independent

Claims 1 and 5 (and claims depending therefrom) patentably distinguish over Mowery and Huang.

In response to the Applicant's argument, the Examiner, the claim limitation does not include said specificity of connection configuration, and thus the applied art means the breadth, and scope of the limitation as presented. Therefore, applicant's argument is not considered persuasive.

Conclusion

10.   Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER A. DALEY whose telephone number is (571)272-3625. The examiner can normally be reached on 9 am. - 4p m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571 272 3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Christopher A Daley/
Examiner, Art Unit 2111

/Khanh Dang/
Primary Examiner, Art Unit 2111